REMARKS

Claims 17-25 are presented for further examination. All of the pending claims have been amended.

In the Office Action mailed October 23, 2002, the Examiner objected to claims 21-25 because of informalities, rejected claims 17-25 under 35 U.S.C. § 112, first paragraph, and claims 18-20 were rejected under 35 U.S.C. § 112, second paragraph as indefinite. With respect to the merits, claims 17-20 and 24 were rejected under 35 U.S.C. § 103(a) as unpatentable over Cogan in view of Pearce, both of record in this application.

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

Claims 21-25 have been amended to overcome the objections raised by the Examiner regarding the informalities therein.

With respect to the rejection of claims 17-25 under 35 U.S.C. § 112, first paragraph, the Examiner first states that the specification "never discloses a vertical DMOS transistor" as recited in claims 17 and 21-25. Applicant respectfully directs the Examiner's attention to Figure 18, which shows a vertical DMOS transistor adapted for use in an integrated circuit. The current flow of the device is from the channel region, vertically down to the N+ varied layer 54, through the buried layer 54 to the N+ "sinker" diffusion 64, and through the N+ "sinker" diffusion 64 to the drain contact 100 on the top surface. The art of record, EP 0747969A1, describes this structure as a quasi-vertical DMOS device.

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The Examiner also objected to the recitation of "the gate has not induced a channel region between the source region and the drain region" as recited in claim 17. This phrase has been deleted.

The Examiner further stated that the specification "never discloses a plurality of insulated gate electrodes formed over the outer portions and inner central portions of the first and second source regions, respectively, as claimed in claim 22." Applicant respectfully directs the Examiner's attention to Figures 14-18 wherein the gate electrodes 84 are shown positioned over the outer portion of the first source region 90 and the inner portions of the second source regions 92, which was recited in original claims 6 and 7. The formation of the first and second source

regions 90, 92 is described on page 10 of the specification as having their edges in alignment with the gate regions 84. Applicant respectfully submits that this recitation is clearly supported by the figures, claims, and specification.

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The rejection under 35 U.S.C. § 112, second paragraph, of claims 18-20 has been traversed by the foregoing amendments to these claims.

Turning to the merits, the disclosed and claimed embodiments of the invention are directed to reducing or eliminating the operational characteristics of parasitic devices associated with a power DMOS structure In an integrated circuit having many other transistors on the same substrate, *i.e.*, a complex integrated circuit. The method of operation claimed herein is dependent on the integrated nature of the vertical DMOS device, as clearly recited in each of the independent claims.

The disclosed and claimed embodiments of the invention are directed to preventing latch-up of the DMOS device when it is in reverse operation as a consequence of the source voltage becoming higher than the drain voltage. Because of the vertical nature of the claimed DMOS device, a parasitic device is created when the DMOS transistor goes in to reverse peroration, which in turn can cause the DMOS transistor to latch up. The method of the present invention prevents or substantially reduces this operational characteristic of the parasitic device.

In contrast, Cogan describes the operation of a "merged" device that consists of a vertical DMOS transistor and a Schottky diode (*see* Cogan, col. 4, lines 25-56). Cogan claims an "improved DMOS transistor" and not an integrated transistor formed in association with a complex integrated circuit. Cogan does not teach or suggest a method of operating a DMOS device having a vertical PNP (or NPN) configuration.

Pearce makes no teaching or suggestion of any conditions wherein the source voltage is above the drain voltage. Moreover, Pearce does not disclose or suggest the driving of inductive loads or the use of H-bridges. Thus, in claim 17, the recitation of the method comprising diverting current from flowing through the body-to-drain pn junction diode of the DMOS transistor to flowing through the Schottky diode that is co-integrated with the DMOS transistor when the metallic source contact becomes more positive than a drain formed by the DMOS transistor by forward conduction voltage of the Schottky diode to reduce the amount of

source current reaching the substrate and substantially reducing operational characteristics of parasitic devices associated with the integrated circuit is not rendered obvious by the combination of Pearce and Cogan.

If one were motivated to combine the teachings of Cogan with Pearce, such combination would fall short of the claimed method. Pearce teaches the use of a pilot transistor to determine current flow through his device. The purpose of the buried layer is to form a low resistance path along the arrows shown in the figures. There is no discussion or suggestion in Pearce of reducing the gain or current flow. There is no discussion whatsoever in Pearce of what would happen if his device went into reverse operation.

OK

Cogan teaches a discreet device having a Schottky diode to prevent turning on of a PN junction. There is no teaching or suggestion of how to operate a vertical DMOS transistor to "*reduce* the amount of source current reaching the substrate." Furthermore, Cogan has no parasitic PNP (or NPN) device because Cogan does not have the claimed substrate of the vertical DMOS transistor. Thus, the combination of Cogan and Pearce fails to teach or suggest a method of reducing the operational characteristics of a parasitic device (PNP or NPN) as does the present method. Applicant respectfully submits that claim 17, dependent claims 18-20, and independent claim 21 are allowable for these reasons.

OK

Claims 22-25 are directed to a similar method wherein the amount of source current reaching the substrate is no more than 3% to 4% of the source current. There is no teaching or suggestion in the combination of Pearce and Cogan of reducing gain and current flow from the source to the substrate to be no more than 3% to 4% of the source current. Applicants submit that claims 22-25 are allowable for this reason as well as for the reasons discussed above with respect to claims 17-21.

not OK

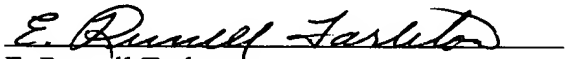
In view of the foregoing, applicant submits that all of the claims in this application are clearly in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

Paolo Menegoli

SEED Intellectual Property Law Group PLLC



E. Russell Tarleton
Registration No. 31,800

ERT:aep

Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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